METHOD TO IMPROVE CACHE CAPACITY OF SOI AND BULK

ABSTRACT

Methods for designing a 6T SRAM cell having greater stability and/or a smaller cell size are provided. A 6T SRAM cell has a pair access transistors (NFETs), a pair of pull-up transistors (PFETs), and a pair of pull-down transistors (NFETs), wherein the access transistors have a higher threshold voltage than the pull-down transistors, which enables the SRAM cell to effectively maintain a logic "0" during access of the cell thereby increasing the stability of the cell, especially for cells during "half select." Further, a channel width of a pull-down transistor can be reduced thereby decreasing the size of a high performance six transistor SRAM cell without effecting cell the stability during access. And, by decreasing the cell size, the overall design layout of a chip may also be decreased.